IN THE DRAWINGS:

By way of a separate letter attached hereto, applicants propose to amend Fig. 6 to includes blocks for providing a virtual clock signal and generating a test pattern. Upon indication of allowance, and with the Examiner's approval, the changes will be incorporated into a new set of formal drawings.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Sitaram YADAVALLI, et al.

Serial No.:	09/531,910	Group Art Unit:	2123
Filed:	March 20, 2000	Examiner:	H. Day

FOR: METHOD AND APPARATUS FOR MODELING AND CIRCUITS WITH ASYNCHRONOUS BEHAVIOR

PROPOSED CHANGES TO THE DRAWINGS

Commissioner for Patents
Mail Stop AF
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed January 20, 2004, applicants propose to amend Fig. 6 to add blocks 66 and 68. With the Examiner's approval, the changes will be incorporated into the formal drawings upon indication of allowance.

If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

April 20, 2004
Date

Paul E. Steiner
Reg. No. 41,326
(703) 633 - 6830

Intel Americas
LF3
4030 Lafayette Center Drive
Chantilly, VA 20151

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

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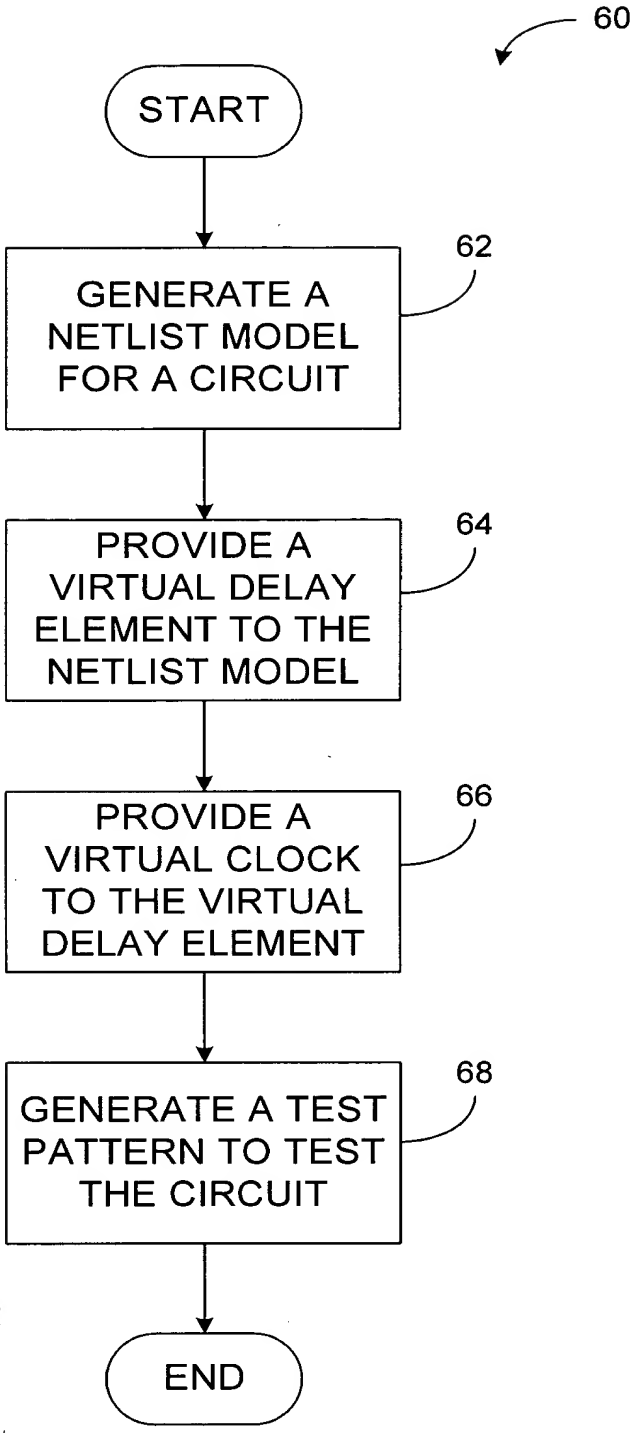

Figure 6